IN THE CLAIMS:

Claim 1 (currently amended): An offset correction circuit to correct DC offset in accordance with a data rate, comprising:

a head to read data at a data rate recorded on a disk;

a detection circuit to detect a thermal asperity signal; and

a filter circuit to respond to said thermal asperity signal in accordance with said recorded data rate.

Claim 2 (original): An offset correction circuit, as in Claim 1, wherein said filter circuit affects said DC offset in accordance with said data rate.

Claim 3 (original): An offset correction circuit, as in Claim 1, wherein said filter circuit is a transconductance circuit.

Claim 4 (original): An offset correction circuit, as in Claim 3, wherein said transconductance circuit shunts current in accordance with said data rate.

Claim 5 (original): An offset correction circuit, as in Claim 3, wherein said transconductance circuit includes a FET to shunt current in accordance with said data rate.

Claim 6 (currently amended): A disk drive system for reading and writing information on a disk, comprising:

a head to read/write information on said disk at a data rate recorded on said disk;

a preamplifier to amplify said information; and

a read channel to process said amplified information, said read channel including:

an offset correct circuit to correct DC offset in accordance with a data rate, said offset correction circuit including:

a detection circuit to detect a thermal asperity signal; and

a filter circuit to respond to said thermal asperity signal in accordance with said recorded data rate.

Claim 7 (original): A disk drive system, as in Claim 6, wherein said filter circuit affects said DC offset in accordance with said data rate.

Claim 8 (original): A disk drive system, as in Claim 6, wherein said filter circuit is a transconductance circuit.

Claim 9 (original): A disk drive system, as in Claim 8, wherein aid transconductance circuit shunts current in accordance with said data rate.

Claim 10 (original): A disk drive system, as in Claim 8, wherein said transconductance circuit includes a FET to shunt current in accordance with said data rate.